Parsa Mirfasihi

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Objective

Electrical and Computer Engineering Master's student seeking internship/full-time opportunities in the VLSI/ASIC design space to apply my expertise in RTL design, verification, and physical implementation to develop efficient and scalable hardware solutions.

Education

San Francisco State University, San Francisco, CA — Jan. 2024 – May 2026

- Masters of Science in Electrical and Computer Engineering – 4.0 GPA
- Graduate Research assistant at Nano Electronics and Computing Research Laboratory (NeCRL) under Dr. Hamid Mahmoodi.

Iran University of Science and Technology, Tehran, Iran — May. 2022

- Bachelor of Science in Electrical Engineering – 3.8 GPA

Relevant Coursework

- Digital VLSI Design(Full-custom – schematic to layout)
- Analog IC Design
- Advanced Digital Design (ASIC RTL to GDS flow)
- Digital Design Verification

Experience

Research Assistant, Nano Electronics & Computing Research Lab (NeCRL) — Jan. 2025 – Present

- Investigated the impact of interconnect parasitics on gate delay in nanoscale circuits by designing and simulating distributed RC networks in 14nm FinFET CMOS. Automated HSPICE data generation and circuit feature extraction with Python to train an in-house ML framework (ML-Net) that selects the optimal reduced RC model with 1% delay deviation from a fully distributed reference. Introduced and validated a novel Double-π model, achieving over 94% classification accuracy across inverter sizes and timing arcs, demonstrating its practicality for accurate and scalable VLSI timing analysis. **(3rd Place - Fall 2025 SoE Showcase)**
- **Submitted to Design Automation Conference (DAC) 2026.**
- **Skills gained**: full-custom VLSI design flow, DRC/LVS verification, parasitic extraction, HSPICE simulation, and timing analysis.

System-Level Power Analysis Engineering Intern — Sep. 2024 – Apr. 2025

Industrial Assessment Center at SFSU – `https://www.iac.sfsu.edu/`

- Led DOE-funded energy audits focused on electrical systems and system-level power analysis.
- Served as audit lead for multiple on-site assessments, overseeing electrical metering, instrumentation, and data validation.
- Collected and analyzed electrical power/load datasets; performed statistical analysis and feature extraction using Python and R.
- Developed system-level power models to identify peak drivers and estimate energy and cost savings.
- Prepared and co-authored technical reports and presentations for client stakeholders and incentive program submissions.

Graduate Teaching Assistant – Part Time, San Francisco, CA — Jan. 2024 – Present

- Assisted instruction and grading for multiple core ECE courses including: Digital Design System/Laboratory, Control Systems, Computer Systems, Linear System Analysis, Operational Amplifier System Design, Communication Systems, and Introduction to Microcontrollers.

Projects

Full Custom 16x8 SRAM Block in 14nm FinFET CMOS

- Iteratively designed and implemented a 16x8 SRAM module in 14nm FinFET CMOS technology with the goal of minimizing layout area, access time, and active power while meeting design constraints. Performed full-custom layout of SRAM cell, address decoder, pre-charge circuit, sense amplifier, and write driver; verified design with DRC/LVS. Conducted pre- and post-layout functional verification to validate correct read/write operation.
- Characterized performance, showing standby power of 1.12 nW, active power of 136 μW @ 1 GHz, and max frequency of 10.2 GHz.

Motion Estimator (ASIC 14nm CMOS)

- Designed and verified a motion estimation engine (16×16 reference block, 31×31 search window) from RTL Verilog through physical layout (GDS) in a 14nm CMOS process. Performed synthesis, static timing analysis, and complete back-end physical design (placement, routing, clock tree synthesis, parasitic extraction, and timing closure).
- Skills gained: ASIC design flow, RTL design and verification, synthesis, static timing analysis, physical design, timing closure.

MIPS-based CPU Design (RTL to FPGA)

- Designed a 32-bit pipelined MIPS CPU in Verilog (Vivado) with full datapath, control logic, ALU, and hazard detection/forwarding for correct pipeline execution. Verified functionality using testbenches and instruction-level simulation, supporting arithmetic, logic, branch, and memory operations. Synthesized and deployed on a Xilinx Basys3 FPGA, demonstrating correct execution of MIPS assembly programs in hardware.

Skills

Programming: C, C++, Python, Perl, TCL, Verilog, Linux/Unix

Tools: Synopsys (Custom Compiler, VCS, Design Compiler, IC Compiler, PrimeTime), Vivado Design Suite,ModelSim, MATLAB

Hardware: Oscilloscope, Xilinx FPGAs, Logic Analyzer, Waveform Generator, Teradyne ATE (J750).

Publications

- ML-Net: Enhanced Interconnect Modeling through Machine Learning-Based Framework and Novel Double-π Networks. *(Submitted to **DAC 2026** – Under Review)*
- Designing and implementing a real-time intelligent system for object identification and classification, *7th Int. Conf. on Technology Development in Iranian Electrical Engineering* (19 June 2022, Tehran, Iran).